Design of an AC Excitation Hall Sensor Front-End System with 12-bit SAR ADC

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Abstract

Hall effect sensors have been utilized in several applications that range from industrial and biomedical. It has been deployed alongside magnetic nano-beads into an assay as part of a protein detection platform. However, the hall voltage can be affected by several interfering noise signals in the form of supply hum, dc offsets, temperature variations, circuit induced noises, etc. A possible method that can reduce the effect of these signals is by utilizing an AC excitation line instead of DC. This was demonstrated on this paper as well as the design of a suitable front-end detecting system with a digital output. Such front-end consisted of a chopper stabilized instrumentation amplifier and a bandpass filter based on PMOS pseudoresistors, while the digital back-end consisted of a 12-bit Successive Approximation Register A/D converter. The system was designed using TSMC 0.18 um 1P6M technology.

Keywords: Hall Effect Sensing, Chopper Stabilized Instrumentation Amplifier, AC Magnetic Field, SAR A/D

I. INTRODUCTION

Hall effect sensors are ubiquitously applied in the industry as proximity sensors, flow rate sensors, tilt sensors, etc. [1], as well as in biotechnology and in medicine such as in magnetic resonance imaging (MRI), treatment of hyperthermia, drug delivery, cell and biological material manipulation and separation [2]. Though several magnetic sensing methods exist, CMOS-based Hall effect sensors have the following benefits as compared to its counterparts, namely: scalability down to several micrometers in size to achieve a relatively high signal-to-baseline ratio on the order of 10–100% for magnetic microbeads using relaxation detection techniques [3]; scalability to yield the maximum hall voltage by making it comparable to the bead size; insensitive to metal layers or parasitic inductances; and requires less extensive calibration procedure. The most common implementations for seminconductor-based Hall-effect sensors are the Magnetic FET (MagFET) and the N-well. The latter however permits more scalability in cell and array size.

A magnetic immunoassay protocol which is based on Hall effect sensing is shown in Fig. 1 [4]. Here, the target analyte is captured by the antibody that has been attached to the functionalized surface of a magnetic sensor. Magnetic beads functionalized with antibodies attaches to the captured analyte, where the amount of captured beads is proportional to the change in magnetic field from a base field provided by the DC excitation lines; this translates to a proportional change in hall voltage.

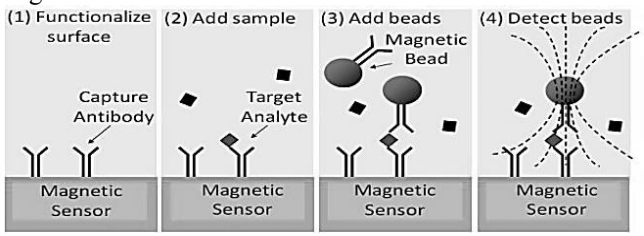


Fig. 1: Magnetic Bead Assay [4]

However, the utilization of a DC magnetic field to yield a DC hall voltage is susceptible to several noise signals namely: temperature variations, power supply hum, DC offsets and readout circuit flicker noise. This leads to inaccuracy in Hall voltage measurements.

To address this, correlated double sampling (CDS) and lock-in approach are commonly used. In CDS, the hall voltage is sampled twice: with and without the magnetic field presence. The difference between these samples is proportional to the concentration of the measurand. Such circuitry uses sample and hold circuits, a 1 bit DAC and an integrator [3]. In the lock-in approach, the AC excitation signal is phase locked to the AC hall voltage then from the quotient of their corresponding magnitudes, the magnetic field variation can be measured. The circuit consists of a coil for generating alternating magnetic field, a magnet for applying perpendicular magnetic field to the sensor, and a Hall sensor connected to a lock-in amplifier to monitor its output voltage [2]. However, both implementations have shown to be rigorous and are relatively complex to implement in a point-of-care device. A third implementation uses the spinning current technique where the hall sensor and bias voltage sides are periodically interchanged producing a high frequency hall voltage; the output has been passed to a chopper stabilized front-end consisting of a chopper circuit, a difference amplifier, hysteresis comparator and control, and high pass filter to remove the low frequency noises and offsets [5]. A possible problem of this would be the introduction of clock feed-through due to the finite inter-electrode capacitances in MOS switches. This couples the switching signals to the hall sensor thereby altering the constant hall bias level and introducing high frequency noise.

In our proposed system, AC excitation is used in the same way as the lock-in approach. This tends to move the bead's responses to a higher frequency making it more distinct and away from low frequency noises. With this stimulus, an AC hall voltage will be generated whose amplitude is proportional to the field variation caused by the bead presence and its amount. However, unlike the lock-in approach, we aim only at detecting the amplitudes of the filtered hall voltage as well as the excitation current to make the algorithm simpler. Issues pertaining to phase difference are projected to be minimal since the operating frequency will not be very high to cause the parasitic capacitors to take effect and alter the hall voltage phase. With the current's intensity fixed, the amplitude of the hall voltage will be reflective of the magnetic field intensity. This is relatively simpler and more straightforward than the lock-in approach. This method has already been explored in our previous work [6].

II. SYSTEM DESIGN AND THEORETICAL FOUNDATION

A. Hall Effect Sensing

In standard CMOS process, the hall sensor is realized using the N-well as shown in Fig. 2. This layer has been used because of its high sheet resistance (due to least doping concentration in

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standard CMOS process) which will improve the sensitivity of the hall sensor [5].

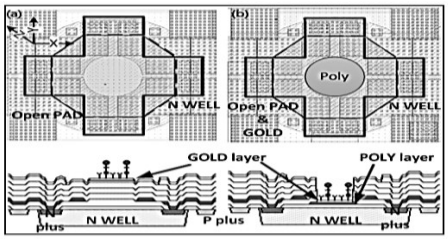


Fig. 2: Hall-effect sensor structure using N-well and gold layer in TSMC Bio-MEMS process

Voltage is applied across the ends of the sensor which generates current as shown in Fig. 3. In the presence of a magnetic field, the charge carriers, in this case, the electrons move across the sides of the sensor perpendicular to both the directions of the field and the current. This is due to the magnetic force applied to a moving charge in the presence of a magnetic field. As a result, a hall voltage is generated.

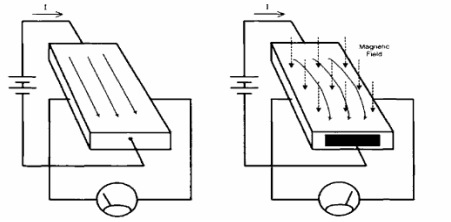


Fig. 3: Principle of Hall Effect

The Hall voltage equation for a typical Nwell hall sensor is given by:

$$V_H = \frac{IB}{q_0 N d} \quad (1)$$

where: V_H is the hall voltage, B is the magnetic field intensity, I is the exciting current amplitude, q_0 is the electron charge; d is the N-well thickness and N is the doping concentration. Since the N-well is lightly doped, the hall voltage is large. Equation (1) can be re-written whenever the magnetic field is an AC sinusoidal wave.

$$V_H \sin(\omega t + \varphi) = \frac{IB sin\sin(\omega t)}{q_0 N d} \quad (2)$$

The presence of phase shift φ is due to the parasitic depletion capacitances present in the N-Well to P-substrate interface. Such can be minimized by choosing an operating frequency in the range of approximately 100 Hz to 100 kHz assuming a depletion capacitance in the range of 100 fF to 2 pF.

B. Hall Sensor in Standard CMOS Process

The structure of the Hall sensor cell is shown in Fig. 4. The cell consists of an exposed area of N-well and a pair of oppositely polarized excitation lines. The directions of current are oriented in such a way that they reinforce the base magnetic field to the sensor. These excitation lines can be implemented using horizontal wires or coils. The size of the hall sensor should be comparable to the size of the target magnetic bead to have optimum detection [1]. If the sensor area is significantly larger than the bead, its magnetic fields will cancel out. Each hall sensor cell is coupled to the output lines or the Bit Lines (BL) via the access transistors. The corresponding digital circuitry to control the hall sensor array is similar to that of SRAM and DRAM as shown in Fig. 5.

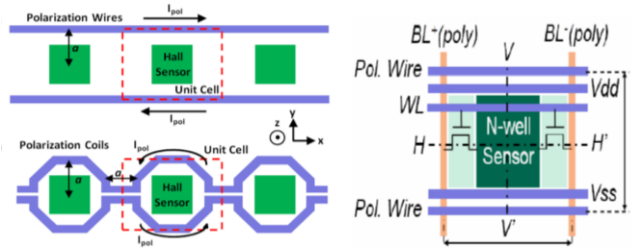


Fig. 4: (a) N-well Hall effect sensor topologies, and (b) Unit sensor cell with access MOS [3]

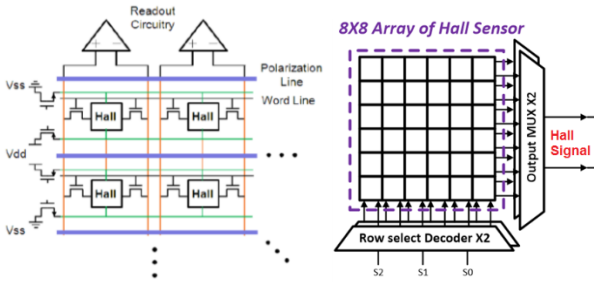


Fig. 5: Array configuration and Digital Controller implementation for the Hall Sensor [3]

C. Chopper Stabilization

For low noise and low offset applications, chopper modulation or stabilization is normally applied. In this method, the signal is up-converted to a high frequency centred on the chopping or sampling frequency prior to passing to the amplifier. Typical MOS-based amplifiers exhibit noise in the form of the flicker (1/f) noise which is dominant in the low frequency, thermal noise and the white noise which is present in all spectrum. These noise signals combine with the input signal within the amplifier. Upon amplification, the signal will then be down-converted back to the low frequency bandwidth, while the low frequency noise signals are up-converted to a high frequency. By using a low pass filter, the amplified low frequency signal is extracted while the up-converted noise signals are attenuated. The chopper stabilization scheme is shown in Fig. 6.

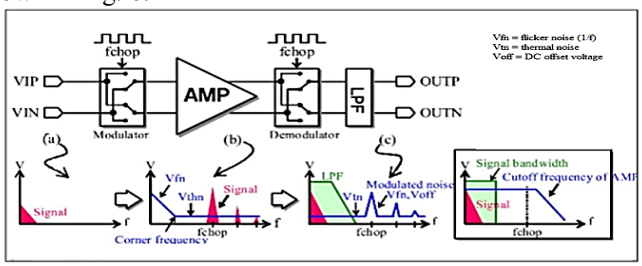


Fig. 6: Chopper stabilization scheme

D. Analog Circuit Front-End

The front-end readout circuit is in the form of a current mode instrumentation amplifier that uses second generation current conveyor blocks. This topology reduces the need for stringent resistor matching as in the case of a voltage-mode 3 opamp IA topology, which allows it to achieve a high common-mode rejection ratio (CMRR). This is essential since the hall voltage is several orders of magnitude smaller than the large background signals and DC offsets that are common to both inputs of the IA. Chopper stabilization has also been incorporated to the IA to reduce the input offset voltages and the low frequency noise inherent in most MOS amplifiers. The complete front-end is shown in Fig. 7.

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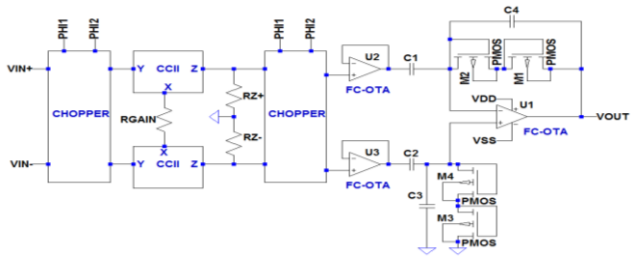


Fig. 7: Complete analog front-end block for hall voltage extraction

The bandpass filter was realized using PMOS pseudoresistors which provide large valued resistances in the range of Giga to Tera Ohms. Such is needed so that the DC component of the chopped signals following the buffer circuits will be attenuated. The use of high resistances permits the reduction of capacitor size, hence can be integrated on-chip. Meanwhile, the excitation line drivers consist of a comparator driving a charge pump circuit or a current starved inverter. This is shown in Fig. 8.

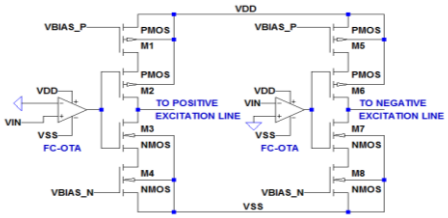


Fig. 8: Excitation line driver circuit

E. The 12-bit Successive Approximation Register (SAR) ADC

A/D converter will be integrated onto the chip along with the analog front-end to reduce any parasitic components and antenna effects. The SAR A/D consists of a sequential logic circuit in the form of a shift register, a comparator, and a D/A converter. The converter was realized using the RC-Hybrid topology to reduce the layout area while maintaining relatively low power dissipation. The functional block diagram of the A/D is shown in Fig. 9.

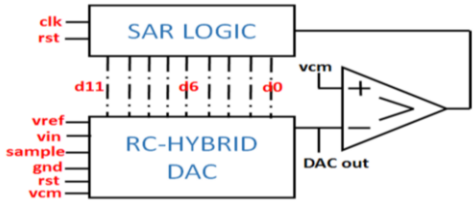


Fig. 9: SAR A/D functional block diagram

The SAR logic begins by placing the MSB to a logic high. This corresponds to an analog output equal to $V_{REF}/2$ which is generated by the D/A. When the output of the comparator is "1", the SAR logic will hold the logic high for MSB. This means that the input in addition to the capacitor voltage value is still less than the common-mode voltage (V_{CM}). During the next clock, the MSB-1 bit is placed on logic high, and the comparison continues till the LSB is reached. The logic levels of all bits after the LSB is the digital code. The structures for the SAR logic, comparator, and the RC-Hybrid D/A are shown in Figs. 10 to 12, respectively. For the voltage comparator a hysteresis voltage of around 10 mV was set, while the resistors and capacitors of the D/A are p+ poly (W/L = 0.5u/50u), mim cap (8u x 8u), respectively. P+ poly has been selected because of its relatively low temperature coefficient and high sheet resistance. The RC-Hybrid D/A consists of a switched resistor string for the 4 LSBs, and a Binary weighted capacitor (BWC) for the 8 MSBs. In this way, a low power, smaller layout area, and low noise can be achieved.

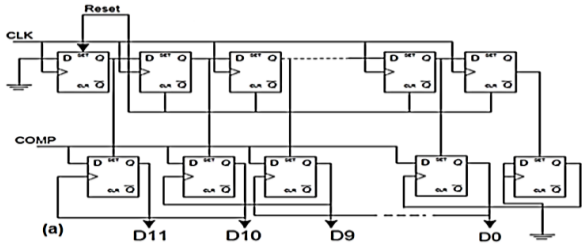


Fig. 10: SAR logic implementation

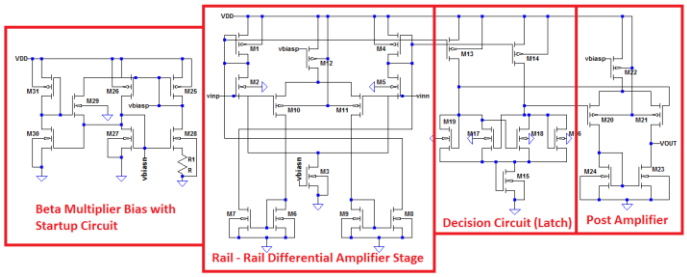


Fig. 11: Voltage comparator implementation

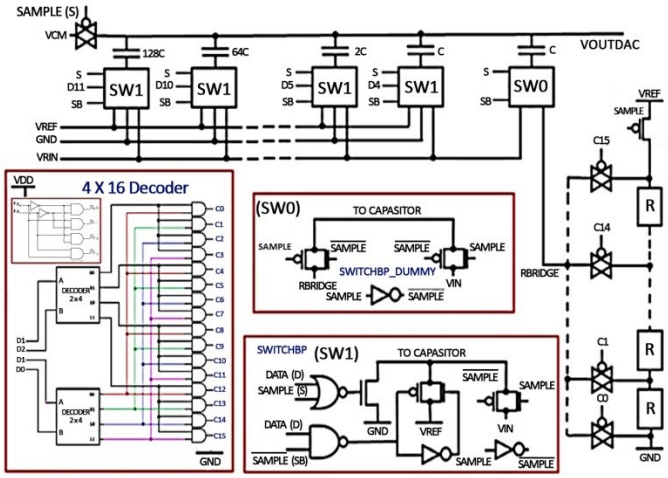


Fig. 12: RC-Hybrid D/A Converter

III. RESULTS AND DISCUSSION

A. Chip test results

We have fabricated a test chip using TSMC 0.18um 1P6M process which contains a 1 x 4 hall effect sensor as shown in Fig. 13. Each sensor cell has a 4 um x 4 um area. We then setup a test-bench to extract the hall voltage as shown in Fig. 14.

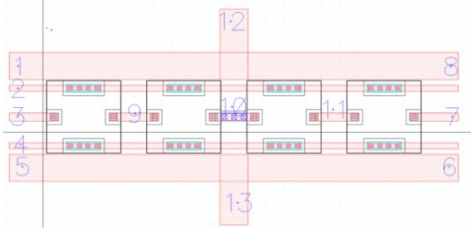


Fig. 13: Fabricated 1 x 4 Hall sensor array

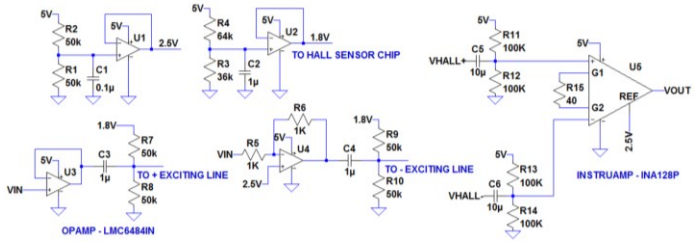


Fig. 14: Test bench for extracting the hall voltage with the bipolar excitation line generators

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We have utilized a signal source with a frequency equal to 723 Hz which is free from any harmonics of common noise sources such as EMI and supply hum. FFT was used to extract the RMS voltage variation with respect to increasing excitation current intensity. It was observed that the hall voltage behaves almost linearly with the excitation current level as shown in Fig. 15. However, there is no observable summation of hall voltages as the hall sensor outputs are connected in series. This could be due to a broken link between the series elements.

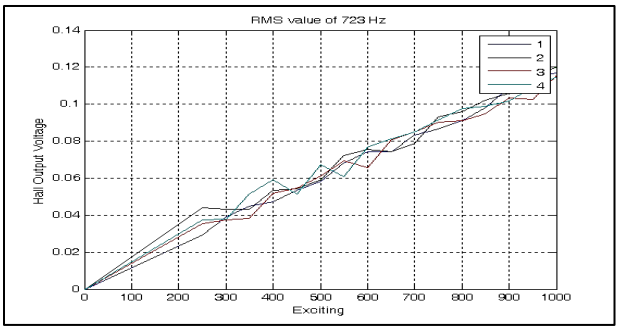


Fig. 15: Extracted RMS voltage for different excitation levels demonstrating the relatively linear response between excitation intensity and hall voltage

B. Analog Front-End Simulation Results

The IA has achieved a high CMRR which is ~100 dB as shown in Fig 16. It also has programmable gain until 30 dB using the matched R_Z resistors. With a significant differential gain and a high CMRR, the differential hall voltage that range from about 100 uV to 1 mV can be extracted effectively. Meanwhile, the bandpass filter has a relatively consistent frequency response for the five corner cases with cut-offs at approximately 5 Hz to 10 kHz. The bandwidth can be tuned by adjusting the dimensions of the PMOS pseudoresistors. The noise contribution of the filter is minimal since it is dominant in the low frequencies (1/f noise) which is not in the band of the hall voltage frequency. Furthermore, the hall voltage will have a total gain of ~50 dB after the filter which will make the Signal – Noise Ratio in the vicinity of 50 - 60 dB. The output referred noise for the five corner cases are shown in Fig. 19.

The simulation results of the complete analog front-end are shown in Figs. 20 - 22. It is evident from the results that the chopper-stabilized IA is functional for the five corner cases since the input voltage can still be extracted with high quality, minor phase shifts and amplitude reductions.

The excitation current driver circuit was able to pump more current onto the load through the charge pump circuit formed by the external MOS devices in Fig. 8. It was able to provide a current amplification factor of about 1000 A/A as shown in Fig. 23 for the five corner cases.

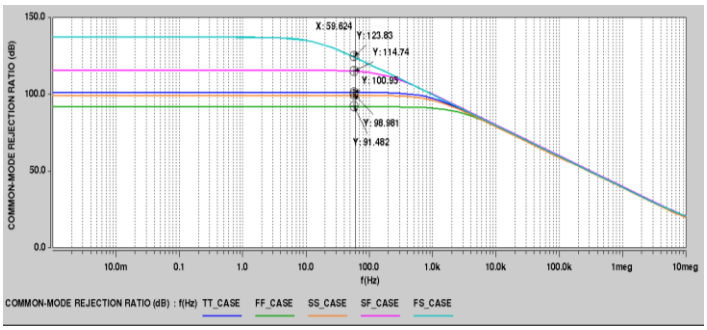


Fig. 16: IA's CMRR for the five corner cases

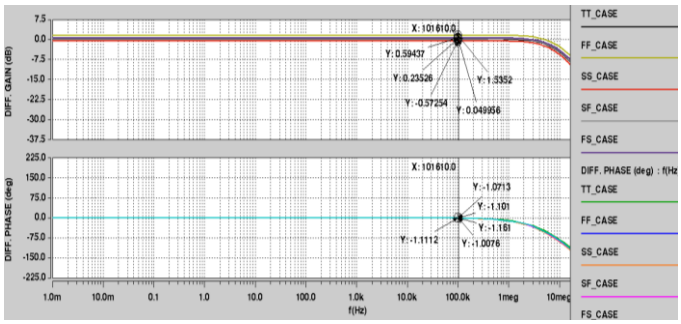


Fig. 17: IA's Unity differential gain frequency response for the five corner cases showing the usable excitation frequency for min. phase error.

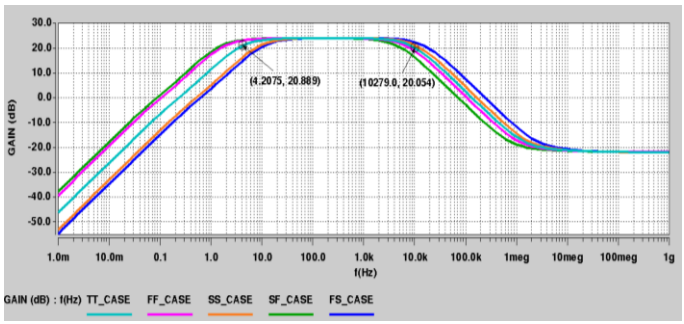


Fig. 18: Bandpass filter's frequency response for the five corner cases

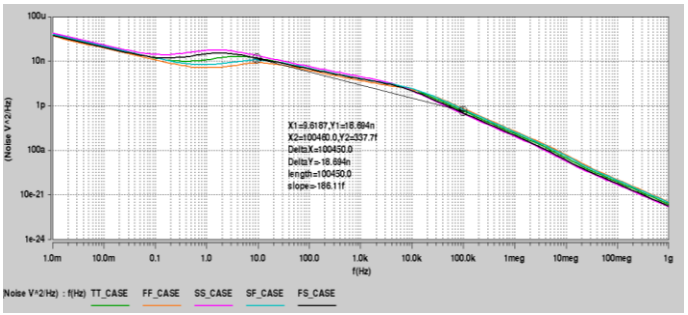


Fig. 19: Bandpass filter's output referred noise spectra for the five corner cases

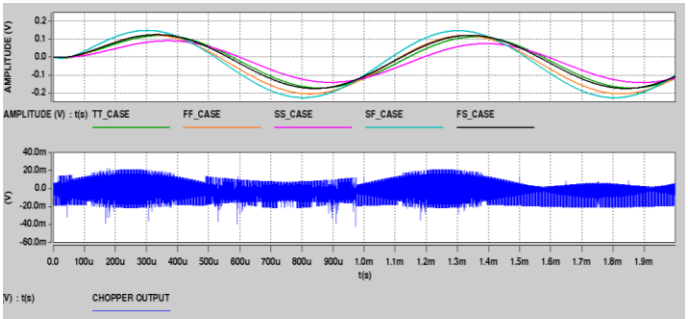


Fig. 20: Chopper stabilized IA filtered output for the five corner cases (top), and the chopped output prior to filtering (bottom) (the input frequency is set at 1kHz and 10 mVpk)

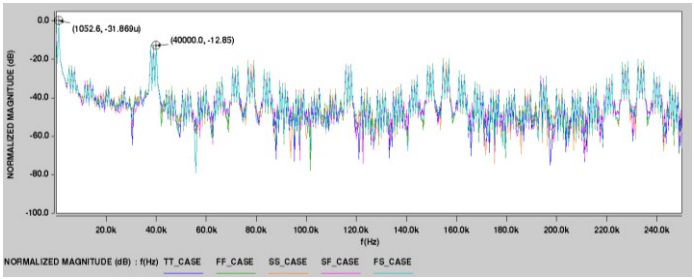


Fig. 21: Normalized FFT results of the chopped output prior to filtering

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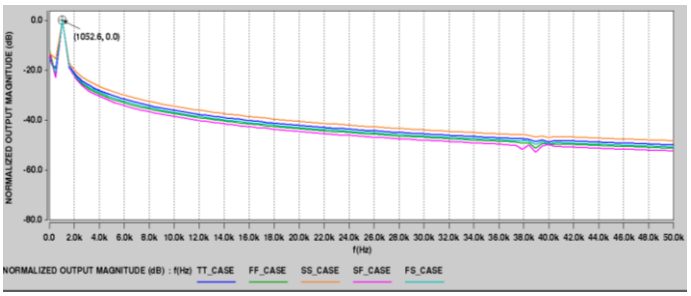


Fig. 22: Normalized FFT results of the filtered output. The SNR is around 20 dB which is a sufficient margin from noise

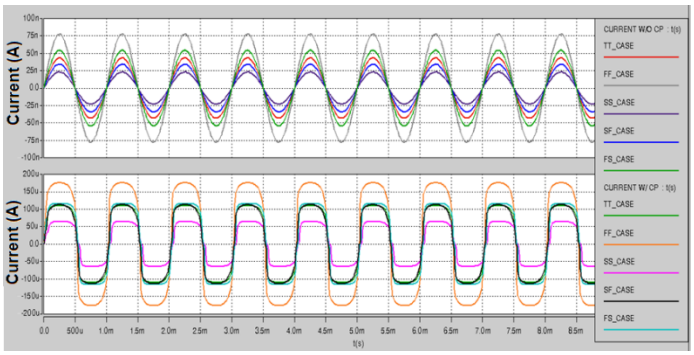


Fig. 23: Differential excitation current with (bottom) and without (top) charge pump for the five corner cases

C. SAR A/D Converter Simulation Results

The voltage comparator has achieved a differential gain of ~600 V/V which is sufficient to latch to either "1" or "0", and has a a hysteresis voltage of 10 mV as shown in Fig. 24. The 12 bit SAR A/D has achieved an INL and DNL in the range of -1 to +2 LSB as shown in Fig. 25. A sample successive approximation step is shown in Fig. 26 which confirms the functionality of the designed A/D converter. Table I summarizes the performance specifications of the designed analog front-end with digital back-end which can be used for Hall Effect Sensing applications using an AC excitation.

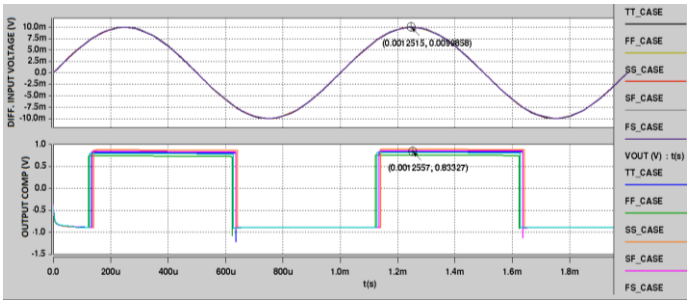


Fig. 24: Voltage comparator transient response showing the hysteresis voltage of 10 mV and a differential gain of ~600 V/V.

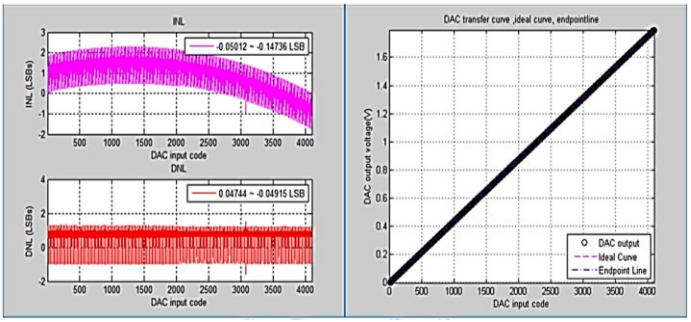


Fig. 25: D/A Converter Integral and Differential Non-Linearities (INL and DNL) and the VOUT vs Digital Code Plot

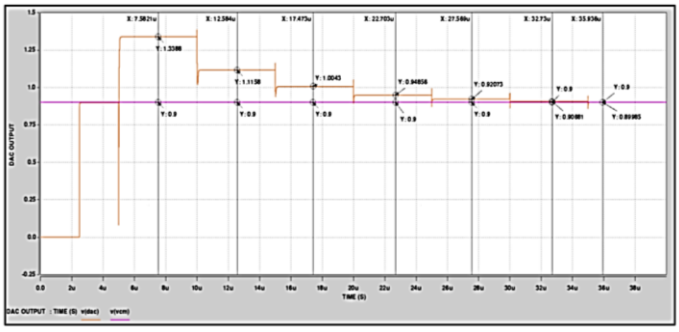


Fig. 25: Successive approximation steps of the D/A where the output converges to the input (sampling rate = 250 kHz)

TABLE I: FRONT-END SYSTEM SPECIFICATIONS

Performance Specification	Value
Technology	TSMC 0.18 um 1P6M
Supply Voltage	+/- 0.9 V
Max. Excitation Bipolar Differential Current Level	+/- 100 uA
Front-End IA Structure	Chopped Current-Mode IA using CCII in Fully Differential Mode
Front-End IA cut-off frequcncy	100 kHz (~1 deg. Phase shift)
Front-End IA maximum programmable differential gain	30 dB
Bandpass Filter bandwidth	10 kHz
A/D Resolution	12 bit
A/D Sampling Frequency	250 kHz to 1 MHz
DC Offset Cancellation	-20 dB
Power Dissipation	< 1 mW (inclusive of A/D converter)

IV. CONCLUSION AND RECOMMENDATIONS

This work was able to demonstrate the functionality of an AC excitation line to generate an AC magnetic field and, ultimately, an AC hall voltage. In this way, the hall voltage may be filtered out from a complex signal that is dominated largely by noise and offset voltages. Such approach is straight-forward and less prone to errors since there is no need for more complex signal processing schemes as in the case of correlated double sampling (CDS) and lock-in amplifier; Phase shift can be minimized by operating at mid-frequency, hence does not require any phase lock-in. We were also able to design a suitable analog front-end and digital back-end that can accompany the use of an AC excitation line. We have presented a new chopper stabilized instrumentation amplifier (IA) and differential input bandpass filter pair which can be used for other low offset signal acquisition. We have also designed a low quantization error ADC dissipating a low power and consumes a lesser area budget with the use of an RC-Hybrid topology.

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